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REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1-17 will remain in the application.

Claims 1 and 2 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada et al. (US 6,225,846), hereinafter Wada, in view of Fujita et al. (US 6,215,159), hereinafter Fujita.

Claims 3-17 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada in view of Fujita and further in view of Rossi et al. (US 6,069,513), hereinafter Rossi.

Applicants respectfully traverse these rejections.

Applicants teach a dynamic bus repeater circuit with an improved noise margin of Vcc/2. This noise margin is closer to that of a static bus repeater than standard dynamic repeaters which may have a noise margin only slightly higher than the threshold voltage of the input transistor. The bus repeater is a dynamic circuit, i.e., it is clocked and has a pre-charge stage in which the value on the input node does not affect the output, and an evaluation stage in which the value on the input does affect the output.

Wada discloses static voltage divider circuit (4), which contains no clocked inputs. Rather than improving the noise margin of a dynamic bus repeater circuit, the voltage divider is provided to reduce the threshold voltages of the inverters (1) and (2) to improve switching speed (col. 4, ll. 60-64).

The circuit (4) disclosed in Wada is not a dynamic bus repeater circuit, but rather a voltage divider circuit. The action characterizes L6 as an input gate and transistor P3 as an input transistor. However, the node L6 is not even connected to the input node L1 in Figure 1, but rather the output node L4. Accordingly, transistor P3 cannot be considered an input transistor.

> "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." MPEP 2143.01 citing In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

The voltage divider is a static circuit. Its proper operation requires that transistors P4 and N4 are always on (col. 4, ll. 10-20). Clocking the input gates to these transistors would make the circuit unsuitable for its intended purpose.

Fujita discloses a clocked circuit, however, since modifying the voltage divider circuit to have clocked input

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gates at transistors P3 and N4 would make the circuit unsuitable for its intended purpose, this combination is improper.

Rossi discloses a flip flop input stage.

None of Wada, Fujita, and Rossi teaches or suggests, either alone or in combination, a dynamic bus repeater with a noise margin of Vcc/2. Accordingly, Applicants submit that independent claims 1 and 11 and their dependencies are allowable.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 10, 2002

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Version with markings to show changes made

In the specification:

Paragraph **[0011]** has been amended as follows:

Figure 2 is a circuit diagram of an exemplary dynamic driver 200. The driver includes a domino gate 202 and an inverter 204. In the pre-charge phase, the Φ1 clock signal is LOW. PMOS transistor 206 is turned on, [proving] providing a path from Vcc, and NMOS transistor 208 is turned off, closing the path to Vss. This pulls intermediate node 210 HIGH, which is inverted to a LOW signal by the inverter 204. The LOW pre-charge signal propagates through the bus line, pre-charging the output nodes of the inverters 110, FF 114, and dynamic repeater 120.

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Applicant : Mark A. Anders, et al.
Serial No. : 09/895,278
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Examiner : Dana Farahani

FACSIMILE COMMUNICATION

Title : DYNAMIC BUS REPEATER WITH IMPROVED NOISE TOLERANCE

Commissioner for Patents
Washington, D.C. 20231

Sir:

Attached to this facsimile communication cover sheet is a Response, faxed this 10th day of July, 2002, to Group 2814, the United States Patent and Trademark Office.

Respectfully submitted,

Date: July 10, 2002

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